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	Nazarian et al., U.S.S.N. 08/626,043, CLOCK DISTRIBUTION ARCHITECTURE AND METHOD FOR HIGH SPEED CPLDS, filed on April 1, 1996.													
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	Babar Raza et al., U.S.S.N. 08/587,659, CIRCUIT FOR HIGH SPEED SERIAL PROGRAMMING OF PROGRAMMABLE LOGIC DEVICES, filed on January 17, 1996.													
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